"[t]he method of claim 23, wherein the step of electrically isolating comprises the step of growing a gate oxide layer within a portion of the conductive layer."

This claim is supported in the specification at least at paragraph [0044] which recites, in part, "[t]he gate oxide 618 growth begins at the surface of the die 604, and develops both into and above the substrate."

35 USC § 102

Komuro:

Claims 14-17 are not invalid as anticipated by Komuro. Komuro does not disclose at least the following limitations of Claims 14-17:

"wherein said surface comprises a doped semiconductor area separated from a second doped semiconductor area by an unbroken insulator area disposed above the semiconductor die."

Kubota:

Claims 19-20 and 23-27 are not invalid as anticipated by Kubota. Kubota does not disclose at least the following limitations of amended Claims 19 and 20:

". . . etching at least said shielding element, thereby forming a surface with both conducting layers and the at least one shielding element"

Kubota does not disclose at least the following limitations of amended Claims 23-25 or 26-27:

". . . etching a trough in the first portion of the conductive layer."

35 USC § 103

Claim 18 is not invalid as obvious over Komuro in view of Kubota. Neither Komuro nor Kubota, alone or in combination disclose, teach or suggest at least the following limitations of Claim 18:

"wherein said surface comprises a doped semiconductor area separated from a second doped semiconductor area by an unbroken insulator area disposed above the semiconductor die."

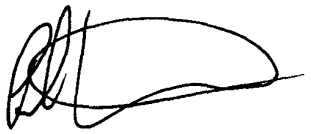
New Claims

Applicant respectfully submits that new Claims 28-35 are fully supported in the specification and are not invalid as anticipated by either Komuro or Kubota and are not unpatentably obvious over either one of Komuro or Kubota in view of the other.

CONCLUSION

Claims 14-17 are not anticipated by Komuro. Claim 18 is not unpatentably obvious over Komuro in view of Kubota. Claims 19-20 and 23-27 are not anticipated by Kubota. The Applicant therefore requests reconsideration of the rejections of Claims 14-20 and 23-27 as set out in the Office Action mailed November 29, 2002. The Applicant respectfully believes that new Claims 28-34 are not invalid over Komuro or Kubota, alone or in combination. The Applicant therefore respectfully requests that the Examiner place the application in condition for allowance.

Respectfully submitted,



Dated: February 24, 2003

Peter J. Reitan
Registration No. 48,603

Law Offices of Larry K. Roberts, Inc.
P.O. Box 8569
Newport Beach, CA 92658-8569
Telephone (949) 640-6200
Facsimile (949) 640-1206

VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

15. (Amended) The process of claim 14, wherein the step of forming at least an insulating layer [on said first doped semiconducting layer] comprises growing a gate oxide layer.

16. (Amended) The process of claim 15, wherein the step of forming at least an insulating layer [on said first doped semiconducting layer] further comprises depositing a gate electrode layer.

19. (Amended) A process of manufacturing a multi-layered integrated circuit, comprising:

forming one or more conducting layers;

forming at least one shielding element isolating at least part of said one or more conducting layers;

etching at least said shielding element, thereby forming a surface with both conducting layers and the at least one shielding element;

further processing said one or more conducting layers.

23. (Amended) A method of inhibiting delamination of a cavitation layer in a multi-layered integrated circuit comprising the steps of:

forming a conductive layer;

electrically isolating a first portion of the conductive layer from a second portion thereof with a shielding element; [and]

depositing the cavitation layer over portions of the first portion and the second portion, and over the shielding element; and

etching a trough in the first portion of the conductive layer.

24. (Amended) The method of claim 23, wherein the step of electrically isolating comprises the step of growing a [field] gate oxide layer within a portion of the conductive layer.

25. (Amended) The method of claim 24, further comprising the step of depositing a polycrystalline silicon layer over the [field] gate oxide layer.